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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,297	07/30/2003	Richard W. Adkisson	200208008-1	9719

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EXAMINER	
BENGHUZZI, MOHSIN M	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,297	ADKISSON, RICHARD W.	
	Examiner M. B.	Art Unit	
	Mohsin (Ben) Benghuzzi	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12,14-18 and 20-24* is/are rejected.

7)☐ Claim(s) *11, 13, 19, 25, 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *July 30, 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *July 30, 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 26 is objected to because of the following: The claim is a method claim that depends from the system claim 20. Examiner believes that this is an unintentional error on applicant's part. The word 'method' should be replaced with 'computer system.' Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10, 12, and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogl et al. (US 6,188,286) in view of Bogdan (US Pub 2004/0028165).

1) Regarding claim 1:

Hogl et al. discloses a system for maintaining a stable synchronization state in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second

clock signals having a ratio of N first clock cycles to M second clock cycles, where N/M $\geq$ 1, comprising:

a first circuit portion operable to generate a load signal indicative of a known acceptable state from which a cycle may be loaded (Column 3 Line 63 to Column 4 Line 7, wherein, 24 in Fig. 3 is interpreted to be the first circuit portion);

a second circuit portion in communication with said first circuit portion, said second circuit portion operating to generate a lock signal indicative of a tolerable tracked skew between said first clock signal and said second clock signal (Column 4 Lines 26-31, wherein, the phase alignment circuit is interpreted as the second circuit portion).

Hogl et al. discloses a third circuit portion, operating responsive to said load signal and said lock signal, for generating a synchronization stable state signal indicative of locking between said first clock signal and said second clock signal (Column 4 Lines 2-7, wherein, the slave device is interpreted as the third circuit portion). Hogl et al. does not disclose a third circuit portion, operating responsive to a zero skew point indicator, for generating a synchronization stable state signal indicative of locking between said first clock signal and said second clock signal. However, Bogdan discloses a third circuit portion, operating responsive to a zero skew point indicator, for generating a synchronization stable state signal indicative of locking between said first clock signal and said second clock signal (Page 3, Lines 2-5 of claim 2).

It is desirable that the circuit of Hogl et al. has a zero skew point indicator as one of its inputs. A zero skew, or a phase difference of zero, is a clear indication that a first

and a second signal are locked in phase, and therefore, synchronized. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include, as Bogdan teaches, a zero skew point indicator as one of the inputs to the third circuit portion of Hogl et al. in order to be able to identify occurrence of phase lock of a first and second signals, and therefore, occurrence of synchronization.

2) Regarding claim 2:

Bogdan further discloses, further comprising a synchronizer configuration interface in communication with each of said first circuit portion, said second circuit portion and said third circuit portion, wherein said synchronizer configuration interface is operable to provide a configuration signal indicative of a skew tolerance between said first clock signal and second clock signal (Page 3, Lines 3-6 of claim 14).

3) Regarding claim 3:

Hogl et al. further discloses, further comprising a synchronizer configuration interface in communication with each of said first circuit portion, said second circuit portion and said third circuit portion, wherein said synchronizer configuration interface is operable to provide a configuration signal indicative of a latency value with respect to at least one of said first clock signal and said second clock signal (Column 3 Lines 5-9, Column 5 Line 65 to Column 6 Line 4, and Column 6 Lines 36-42, wherein, delay is interpreted to be equivalent to a latency value).

4) Regarding claim 4:

Hogl et al. further discloses, wherein said first circuit portion comprises a cycle and sequence generator (Column 3 Line 63 to Column 4 Line 7, wherein, 24 in Fig. 3 is interpreted to be the cycle and sequence generator).

5) Regarding claim 5:

Hogl et al. further discloses, wherein said first circuit portion generates said load signal in response to a stable state signal (stable_state) generated by said third circuit portion and a synchronous rising edge signal (sync_redge) generated by a synchronizer pulse detector (Column 3 Line 63 to Column 4 Line 7, wherein, 24 in Fig. 3 is interpreted to be the first circuit portion).

6) Regarding claim 6:

Hogl et al. further discloses, wherein said first circuit portion generates said load signal in response to a stable state signal (stable_state) generated by said third circuit portion, a synchronous rising edge signal (sync_redge) generated by a sync pulse detector, a sampled rising edge signal (syncb0_cr) generated by a sampling block, a sampled falling edge signal (syncb0_cf) signal generated by said sampling block, and phase detection signals (pd_b_cr and pd_b_cf) provided by a phase detector (Column 3 Line 63 to Column 4 Line 7, wherein, 24 in Fig. 3 is interpreted to be the first circuit portion, and Column 5 Lines 32-40).

7) Regarding claim 7:

Hogl et al. further discloses, wherein said second circuit portion comprises a skew state detector (Column 4 Lines 26-31, wherein, the phase alignment circuit is interpreted as the skew state detector).

8) Regarding claim 8:

Hogl et al. further discloses, wherein said lock signal is generated in response to coincident rising edges of said first clock signal and said second clock signal (Column 4 Lines 55-58 and Column 6 Lines 23-48).

9) Regarding claim 9:

Hogl et al. further discloses, wherein said lock signal is generated in response to a zero sequence state signal (seq_state=Z) provided by a precision sequence detector (Column 2 Lines 10-17, wherein, it is clearly understood that when there exist no phase difference, the difference voltage, V_VCO, generated .by the phase detector is zero, and therefore, control voltage produced is also zero).

10)Regarding claim 10:

Hogl et al., as discussed above in claim 1, discloses, wherein said third circuit portion comprises a stable state detector (Column 4 Lines 2-7, wherein, the slave device is interpreted as the stable state detector).

11)Regarding claim 12:

Bogdan further discloses, wherein said lock signal is operable as a zero skew point indicator in a 1:1 ratio mode wherein said N/M=1 (Page 3, Lines 2-5 of claim 2).

12)Regarding claim 14:

Hogl et al. teaches a method for maintaining a stable synchronization state in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, comprising:

generating a load signal indicative of a known acceptable state from which a cycle may be loaded (Column 3 Line 63 to Column 4 Line 7 and 24 in Fig. 3);

generating a lock signal indicative of a tolerable tracked skew between said first clock signal and said second clock signal (Column 4 Lines 26-31).

Hogl et al. teaches, responsive to said load signal and said lock signal, generating a synchronization stable state signal indicative of locking between said first clock signal and said clock signal (Column 4 Lines 2-7). Hogl et al. does not teach, responsive to a zero skew point indicator, generating a synchronization stable state signal indicative of locking between said first clock signal and said clock signal. However, Bogdan teaches, responsive to a zero skew point indicator, generating a synchronization stable state signal indicative of locking between said first clock signal and said clock signal (Page 3, Lines 2-5 of claim 2).

As discussed above in claim 1, it is desirable to have the method of Hogl et al responsive to a zero skew point indicator, generating a synchronization stable state

signal indicative of locking between said first clock signal and said clock signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a zero skew point indicator, as Bogdan teaches, in the method of Hogl et al. in order to be able to identify occurrence of phase lock of a first and second signals, and therefore, occurrence of synchronization.

13)Regarding claim 15:

Hogl et al. further teaches, wherein said load signal is generated in response to a stable state signal (stable_state) and a synchronous rising edge signal (sync_redge) (Column 3 Line 63 to Column 4 Line 7 and 24 in Fig. 3).

14)Regarding claim 16:

Hogl et al. further teaches, wherein said load signal is generated in response to a stable state signal (stable_state) generated by said third circuit portion, a synchronous rising edge signal (sync_redge) generated by a sync pulse detector, a sampled rising edge signal (syncb0_cr) generated by a sampling block, a sampled falling edge signal (syncb0_cf) signal generated by said sampling block, and phase detection signals (pd_b_cr and pd_b_cf) provided by a phase detector (Column 3 Line 63 to Column 4 Line 7 and 24 in Fig. 3).

15)Regarding claim 17:

Hogl et al. further teaches, wherein said lock signal is generated in response to coincident rising edges of said first clock signal and said second clock signal (Column 4 Lines 55-58 and Column 6 Lines 23-48).

16)Regarding claim 18:

Hogl et al. further teaches, wherein said lock signal is generated in response to a zero sequence state signal (seq_state=Z) provided by a precision sequence detector (Column 2 Lines 10-17, wherein, it is clearly understood that when there exist no phase difference, the difference voltage, V_VCO, generated .by the phase detector is zero, and therefore, control voltage produced is also zero).

4. Claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogl et al. (US 6,188,286) and Bogdan (US Pub 2004/0028165) in view of Zerbe et al. (US 6,473,439).

1) Regarding claim 20:

Hogl et al. discloses:

a cycle and sequence generator operable to generate a load signal indicative of a known acceptable state from which a cycle may be loaded (Column 3 Line 63 to Column 4 Line 7, wherein, 24 in Fig. 3 is interpreted to be the cycle and sequence generator);

a skew state detector in communication with said cycle and sequence generator, said skew state detector operating to generate a lock signal indicative of a tolerable treated skew between said first clock signal and said second clock signal (Column 4 Lines 26-31, wherein, the phase alignment circuit is interpreted as the skew state detector).

a stable state detector, operating responsive to said load signal and said lock signal, for generating a synchronization stable state signal indicative of locking

between said first clock signal and said second clock signal (Column 4 Lines 2-7, wherein, the slave device is interpreted as the stable state detector). Hogl et al. does not disclose a stable state detector, operating responsive to a zero skew point indicator, for generating a synchronization stable state signal indicative of locking between said first clock signal and said second clock signal.

Bogdan discloses:

a stable state detector, operating responsive to a zero skew point indicator, for generating a synchronization stable state signal indicative of locking between said first clock signal and said second clock signal (Page 3, Lines 2-5 of claim 2).

As discussed above in claim 1, it is desirable that the stable state detector of Hogl et al. has a zero skew point indicator as one of its inputs. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include, as Bogdan teaches, a zero skew point indicator as one of the inputs to the stable state detector of Hogl et al. in order to be able to identify occurrence of phase lock of a first and second signals, and therefore, occurrence of synchronization.

Hogl et al. and Bogdan do not disclose a computer system having an apparatus for maintaining a stable synchronization state in a programmable clock synchronizer used in effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$. However, Zerbe et al.

discloses a computer system having an apparatus for maintaining a stable synchronization state in a programmable clock synchronizer used in effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$ (Column 1 Lines 26-29).

It is desirable to have a computer system with an apparatus for maintaining a stable synchronization state (see Zerbe et al., Column 2 Lines 27-29). Having a computer system with an apparatus for maintaining a stable synchronization state allows for synchronous transmission between separate computer system components, and as a result of using such transmission, data is transmitted between components at the highest rate with the lowest latency. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the computer system of Zerbe et al. include Hogl et al. and Bogdan's apparatus for maintaining a stable synchronization state, in order to allows for synchronous transmission between separate computer system components, and thus, data is transmitted between components at the highest rate with the lowest latency.

2) Regarding claim 21:

Hogl et al. further discloses, wherein said cycle and sequence generator generates said load signal in response to a stable state signal (stable_state) generated by said stable state detector and a synchronous rising edge signal (sync_redge)

generated by a synchronizer pulse detector (Column 3 Line 63 to Column 4 Line 7, wherein, 24 in Fig. 3 is interpreted to be the cycle and sequence generator).

3) Regarding claim 22:

Hogl et al. further discloses, wherein said cycle and sequence generator generates said load signal in response to a stable state signal (stable_state) generated by said stable state detector, a synchronous rising edge signal (sync_redge) generated by a sync pulse detector, a sampled rising edge signal (syncb0_cr) generated by a sampling block, a sampled falling edge signal (syncb0_cf) signal generated by said sampling block, and phase detection signals (pd_b_cr and pd_b_cf) provided by a phase detector (Column 3 Line 63 to Column 4 Line 7, wherein, 24 in Fig. 3 is interpreted to be the cycle and sequence generator, and Column 5 Lines 32-40).

4) Regarding claim 23:

Hogl et al. further discloses, wherein said lock signal is generated in response to coincident rising edges of said first clock signal and said second clock signal (Column 4 Lines 55-58 and Column 6 Lines 23-48).

5) Regarding claim 24:

Hogl et al. further discloses, wherein said lock signal is generated in response to a zero sequence state signal (seq_state=Z) provided by a precision sequence detector (Column 2 Lines 10-17, wherein, it is clearly understood that when there exist no phase difference, the difference voltage, V_VCO, generated .by the phase detector is zero, and therefore, control voltage produced is also zero).

Allowable Subject Matter

5. Claims 11, 13, 19, 25, and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to clearly teach or suggest the system as recited in claim 1 (and the computer system as recited in claim 20), wherein a circuit (a stable state detector) transmits a synchronization stable state signal to a first circuit disposed in a first clock domain. The prior art of record also fails to clearly teach or suggest a third circuit that provides a zero skew point indicator by ANDing a cycle signal provided by a first circuit and a pd_z signal provided by a second circuit.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Richley (US 5,223,755) discloses a delay locked loop for clock synchronization that is capable of aligning a clock signal with a reference signal in the shortest time and without instability.

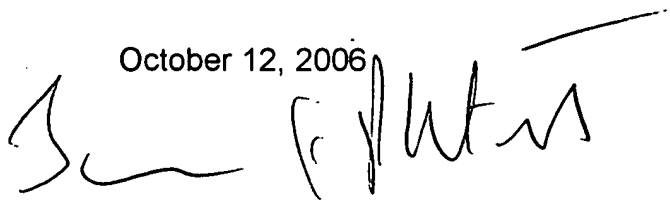
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsin (Ben) Benghuzzi whose telephone number is (571) 270-1075. The examiner can normally be reached Monday through Friday, 8:30am- 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mohsin (Ben) Benghuzzi

October 12, 2006



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